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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,852	12/29/2003	Jaroslaw J. Sydir	Intel-012PUS	2755
	7590 09/03/200 LEY, MOFFORD & D	EXAMINER		
C/O INTELLE	VATÉ, LLC	ZHE, MENG YAO		
P.O. BOX 5205 MINNEAPOLI	=	ART UNIT	PAPER NUMBER	
	,		2195	
			MAIL DATE	DELIVERY MODE
			09/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Applicat	ion No.	Applicant(s)					
Office Action Summary		10/747,8	52	SYDIR ET AL.					
		Examine	r	Art Unit					
		MENGYA	AO ZHE	2195					
	The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply								
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).									
Status									
	Responsive to communication(s) filed	d on 02 June 2008							
•	•	b) This action is :	non-final						
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is								
٥/١	closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.								
Dispositi	on of Claims		,						
· · _		anding in the applier	ation						
•	Claim(s) 1-3,5-21 and 25-30 is/are pending in the application.								
	4a) Of the above claim(s) is/are withdrawn from consideration.								
	5)  Claim(s) is/are allowed. 6)  Claim(s) <u>1-3, 5-21, 25-30</u> is/are rejected.								
· ·		ilea.							
	7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or election requirement.								
·		lion and/or election	requirement.						
Applicati	on Papers								
9)☐ The specification is objected to by the Examiner.									
10)	10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).									
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).									
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.									
Priority ι	ınder 35 U.S.C. § 119								
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>									
2)  Notic 3)  Inform	t(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (P <sup>-</sup> nation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date <u>2/14/08, 6/2/08</u> .	ГО-948)	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal 6) Other:	Oate					

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## **DETAILED ACTION**

1. Claims 1-3, 5-21, 25-30 are presented for examination.

## Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1-3, 5-8, 15-21, 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al., Patnet No. 6,105,053 (hereafter Kimmel) in view of Sihlbom et al., Pub No. 2002/0188885 (hereafter Sihlbom) further in view of Delaney et al., Patent No. 5,996,086 (hereafter Delaney).
- 4. Kimmel and Sihlbom were cited in the last office action.
- 5. As per claims 1, 5, 7-8, 15, 18, 20-21, 25-26, 27-28, Kimmel teaches a multi-processor network system comprising:

a command queue to store commands, the commands comprising a first command associated with a first context (Column 2, lines 2-21: the queue for the root node corresponds to a command queue);

cores comprising a first core and a second core (Column 2, lines 2-7);

same context command queues configured to store commands of a same context, the same-context-command queues comprising a first same –context command queue coupled to the first core and a second same-context-command queue coupled to the second core (Column 2, lines 2-21; Column 9, lines 29-38);

a scheduler configured to received the first command from the command queue (Column 9, lines 56-63; Column 10, lines 34-53).

Kimmel does not specify that the multi-processor system is all contained in one processor, and that multiple cores are embedded on this processor. Furthermore, Kimmel does not specify that each command queue may be a FIFO queue.

However, Sihlbom teaches that the multi-processor system is all contained in one processor, and that multiple cores are embedded on this processor (Abstract, lines 1-2) and each command queue may be a FIFO queue (Para 20) for the purpose of building an optimized processing device.

It would have been obvious to one having ordinary skill in the art to modify the teachings of Kimmel of having a multi-processing system with multiple processors, each with its own queue, with a single processor having a plurality of cores and a FIFO, as taught by Sihlbom, in order to have a single processor having a plurality of cores, each having its own FIFO queue, because it allows for an optimized processing device.

Kimmel in view of Sihlborn does not specifically teach if a first core is idle, determine whether a second core is idle; if the second core is not idle and the second core is processing a second command associated with a second context, determine whether the second context is the same as the first context; and if the second context is the same as the first context, store the first command in the second same-context-command queue.

However, Delaney teaches if a first core is idle, determine whether a second core is idle; if the second core is not idle and the second core is processing a second command associated with a second context, determine whether the second context is the same as the first context; and if the second context is the same as the first context, store the first command in the second same-context-command queue (Abstract; Column 5, lines 1-18: failing corresponds to idling.) for the purpose of continuing execution of threads in case of failure.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Kimmel in view of Sihlborn with if a first core is idle, determine whether a second core is idle; if the second core is not idle and the second core is processing a second command associated with a second context, determine whether the second context is the same as the first context; and if the second context is the same as the first command in the second same-context-command queue, as taught by Delaney, because it allows a thread to continue its execution in the event of failure.

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6. As per claims 3, Kimmel teaches wherein the cores correspond to a first plurality of cores in a first core group and the network processor further comprises: a plurality of core groups; and said command queue corresponds to a first one of a plurality of command queues, each of said plurality of command queues coupled to a corresponding one of said plurality of core groups (Column 2, lines 2-21; Figs 1, 2).

7. As per claims 2, 6, 16-17, 19, Kimmel teaches a multi-processor network system comprising:

a command queue to store commands, the commands comprising a first command associated with a first context (Column 2, lines 2-21: the queue for the root node corresponds to a command queue);

cores comprising a first core and a second core (Column 2, lines 2-7);

same context command queues configured to store commands of a same context, the same-context-command queues comprising a first same –context command queue coupled to the first core and a second same-context-command queue coupled to the second core (Column 2, lines 2-21; Column 9, lines 29-38);

a scheduler configured to received the first command from the command queue (Column 9, lines 56-63; Column 10, lines 34-53).

determine if the queue is full (Column 7, lines 47-63).

Kimmel does not specify that the multi-processor system is all contained in one processor, and that multiple cores are embedded on this processor. Furthermore, Kimmel does not specify that each command gueue may be a FIFO gueue.

However, Sihlbom teaches that the multi-processor system is all contained in one processor, and that multiple cores are embedded on this processor (Abstract, lines 1-2) and each command queue may be a FIFO queue (Para 20) for the purpose of building an optimized processing device.

It would have been obvious to one having ordinary skill in the art to modify the teachings of Kimmel of having a multi-processing system with multiple processors, each with its own queue, with a single processor having a plurality of cores and a FIFO, as taught by Sihlbom, in order to have a single processor having a plurality of cores, each having its own FIFO queue, because it allows for an optimized processing device.

Kimmel in view of Sihlborn does not specifically teach if a first core is idle, determine whether a second core is idle; if the second core is not idle and the second core is processing a second command associated with a second context, determine whether the second context is the same as the first context; and if the second context is the same as the first context, store the first command in the second same-context-command queue.

However, Delaney teaches if a first core is idle, determine whether a second core is idle; if the second core is not idle and the second core is processing a second command associated with a second context, determine whether the second context is

the same as the first context; and if the second context is the same as the first context, store the first command in the second same-context-command queue (Abstract; Column 5, lines 1-18: failing corresponds to idling.) for the purpose of continuing execution of threads in case of failure.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Kimmel in view of Sihlborn with if a first core is idle, determine whether a second core is idle; if the second core is not idle and the second core is processing a second command associated with a second context, determine whether the second context is the same as the first context; and if the second context is the same as the first command in the second same-context-command queue, as taught by Delaney, because it allows a thread to continue its execution in the event of failure.

Delaney does not teach in the case where both cores are idle, the first core still gets assigned to process the command.

However it would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to have at least a core to execute the command in the event that both cores are idle since this gives the command some chance to execute when one of the cores is activated again in the future.

8. Claims 9-14, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimmel et al., Patnet No. 6,105,053 (hereafter Kimmel) in view of Yung, Patent No.

5,592,679 (hereafter Yung), further in view of Sihlbom et al., Pub No. 2002/0188885 (hereafter Sihlbom).

- 9. Yung was cited in the previous office action.
- 10. As per claims 9, 12, 13, 29-30, Kimmel teaches a multi-processor system comprising: (a) a plurality of cryptographic acceleration units (Fig 1A, units 10, 11), each of said plurality of cryptographic acceleration units comprising: (1) a command queue to store one or more commands (Column 2, lines 12-14); (2) a plurality of processors (units 1, 2); (3) a like plurality of same-context command queues, each of said plurality of same context command queues coupled to a corresponding one of said first plurality of processors (Column 2, lines 12-14); an interface, adapted to couple the first node to another node (Fig 1A, units 12, 16).

Kimmel further teaches a medium term scheduler that governs and monitors all nodes in a hierarchy of processors. As of result, Kimmel does not teach multiple schedulers, where each unit has its own scheduler, since the medium term scheduler is able to schedule across all units. More specifically, Kimmel does not specify for multiple schedulers, where each scheduler is coupled to said command queue and to each of said first plurality of processors in said processor group.

However, Yung teaches multiple schedulers, each coupled to each of said first plurality of execution units in said execution unit group (Fig 2, units 241 and 241b; Column 5, lines 49-56) for the purpose of having a local scheduler for each execution units.

It would have been obvious to one having ordinary skill in the art at the time of the applicant's invention to modify the teachings of Kimmel, where a single scheduler is distributed across multiple units so that it act as a scheduler for each unit of processors with multiple schedulers, each coupled to each of said first plurality of execution units in said execution unit group, as taught by Yung, so that each scheduler is coupled to a processor group for the purpose of having a local scheduler for each execution units.

Kimmel in view of Yung does not specify that the multi-processor system is all contained in one processor, and that multiple cores are embedded on this processor. Furthermore, Kimmel in view of Yung does not specify that each command queue may be a FIFO queue.

However, Sihlbom teaches that the multi-processor system is all contained in one processor, and that multiple cores are embedded on this processor (Abstract, lines 1-2) and each command queue may be a FIFO queue (Para 20) for the purpose of building an optimized processing device.

It would have been obvious to one having ordinary skill in the art to modify the teachings of Kimmel in view of Yung of having a multi-processing system with multiple processors, each with its own queue, with a single processor having a plurality of cores and a FIFO, as taught by Sihlbom, in order to have a single processor having a plurality of cores, each having its own FIFO queue, because it allows for an optimized processing device.

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11. As per claim 10, Kimmel teaches a global queue having an input adapted to receive commands directed toward at least one of said plurality of cryptographic acceleration units and having an output; and a global scheduler having an input coupled to the output of said global queue and having an output adapted to provide a data path to each of said plurality of cryptographic acceleration units (Column 10, lines 34-55). Yung also teaches a global queue (Column 5, lines 29-43).

12. As per claims 11, 14, Kimmel teaches wherein said plurality of processors form a first processor group and wherein the processor further comprises a plurality of processor groups, each of plurality of core groups coupled to said global scheduler (Fig 1A, Column 5, lines 29-43).

## Response to Arguments

- 13. Applicant's arguments filed on 6/2/2008 have been fully considered but are not persuasive.
- 14. In the remark, the applicant argued that:
  - i) Claims 7-14 does not teach units that are specifically cryptographic acceleration units.
- 15. The Examiner respectfully disagree with the applicant. As to point:

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i) The applicant did not define what a cryptographic acceleration unit is except merely stating in the claim that it comprised a series of components.

Kimmel teaches all those components (see rejection above), and therefore, it is considered to be a cryptographic acceleration unit.

## Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MENGYAO ZHE whose telephone number is (571)272-6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00 EST.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Li B. Zhen/ Primary Examiner, Art Unit 2194